

### General Description

The MP8040 and MP8041 (MP804x) are general purpose, high frequency half bridge power drivers capable of driving a 9A load. Both devices integrate both top and bottom N-channel MOSFET power switches and are fully protected from both sourcing and sinking current by a preset cycle-by-cycle current limit. Both devices have a wide input voltage range with the MP8040 range from 7.5V to 25V and the MP8041 7.5V to 32V.

The MP804x features a low-current shutdown-mode, input under-voltage protection, thermal shutdown, and fault flag signal output. They both interface with standard logic signals and are available in small 8-lead SOIC package.

### Ordering Information

Part Number *	Package	Temperature
MP8040DN	SOIC8 w/Exposed Pad	-40 to + 85°C
MP8041DN	SOIC8 w/Exposed Pad	-40 to + 85°C

\* For Tape & Reel use suffix - Z (i.e., MP8040DN-Z)

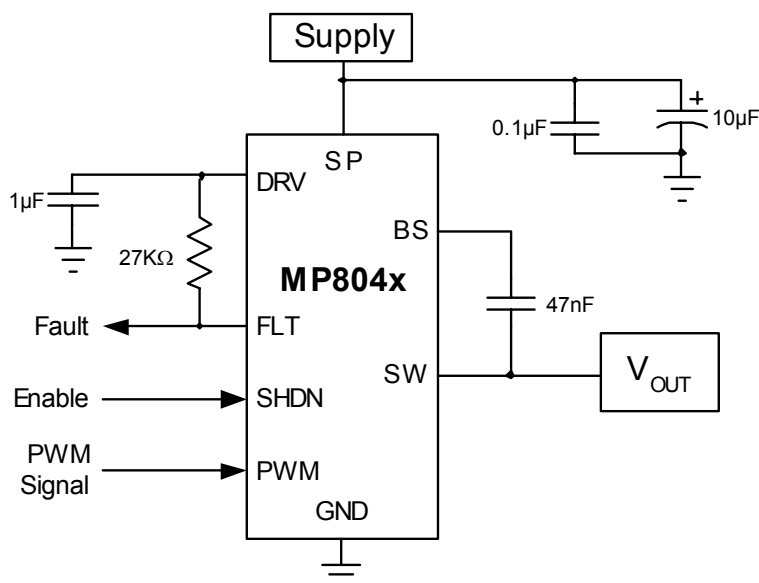
### Features

- +/- 9A Peak Current Output
- +/- 4.25A Continuous Current Output
- Wide Input Voltage Range
  - MP8040: (7.5 to 26V)
  - MP8041: (7.5 to 30V)
- High Audio Output Power
  - MP8040: 25W/4Ω/10% Single Ended
  - MP8040: 70W/4Ω/10% Full Bridge
- Up to 1.2MHz Switching Frequency
- Protected Integrated Power 100mΩ Switches
  - Designed Switch Dead time of 30ns
  - All Switches Current Limited
  - Internal Under-voltage Protection
  - Internal Thermal Protection
- 1μA Standby Mode
- True 2-Quadrant Operation
  - Sources and Sinks Current
- Fault Indicator Output

### Applications

- Full or Half Bridge DC-DC Switching Regulator
- Class D Audio Driver
- Motor Driver

Figure 1: Typical Application Circuit



### Absolute Maximum Ratings (Note 1)

SP Supply Voltage ( $V_{SP}$ ) (MP8040)	-0.3V to 26V
SP Supply Voltage ( $V_{SP}$ ) (MP8041)	-0.3V to 36V
SW Pin Voltage	-0.3V to $V_{SP}$
SW to BS	-0.3V to 6V
Voltage at All Other Pins	-0.3V to 6V
Storage Temperature	-55°C to +150°C

### Recommended Operating Conditions (Note 2)

SP Input Supply Voltage ( $V_{SP}$ ) (MP8040)	7.5 V to 25V
SP Input Supply Voltage ( $V_{SP}$ ) (MP8041)	7.5 V to 32V
Peak Output Current	9A Maximum
Operating Temperature	-40°C to +85°C

### Package Thermal Characteristics (Note 3)

Thermal Resistance $\Theta_{JA}$ (SOIC8-EP)	50°C/W
Thermal Resistance $\Theta_{JC}$ (SOIC8-EP)	8°C/W

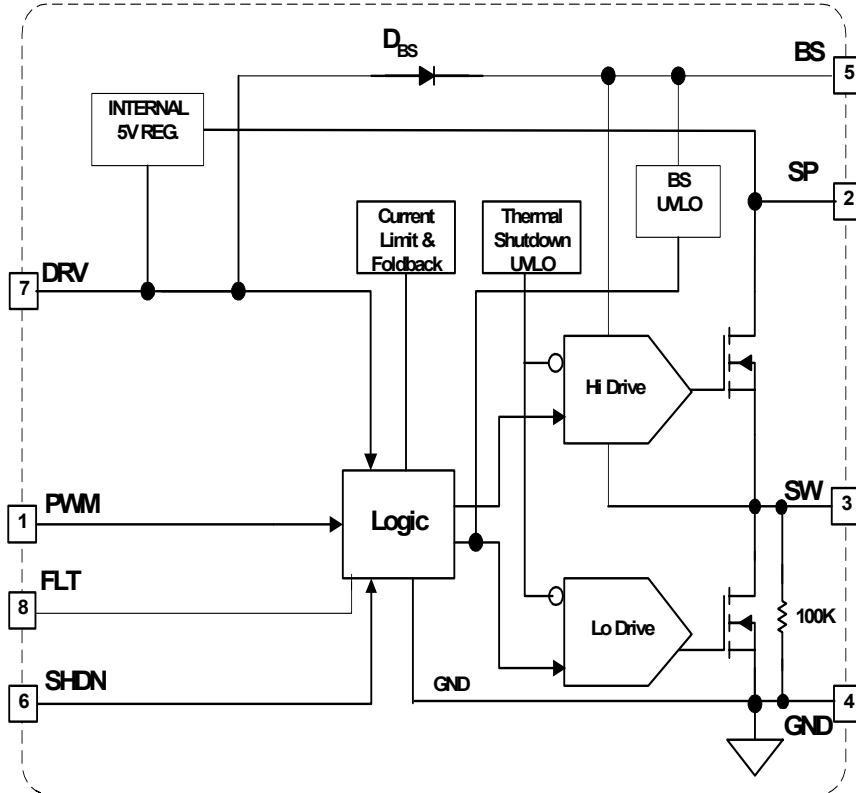
### Electrical Characteristics ( $V_{SP} = 12V$ , $V_{SHDN}=0V$ , $T_A = 25^\circ C$ , unless specified otherwise)

Parameters	Condition	Min	Typ	Max	Units
SP Operating Current			1.5	2.5	mA
SP Shutdown Current	$V_{SHDN} = 2V$		2.5	10	$\mu A$
BS Shutdown Current	$V_{SP} = 7.5V$ , $V_{SHDN} = 2V$		1		$\mu A$
DRV Voltage			5.5		V
SHDN, SP Threshold Low				1	V
SHDN, SP Threshold High		2			V
SHDN, SP Input Bias Current			1		$\mu A$
SW On Resistance	$V_{SP} = 7.5V$ , High-Side and Low-Side		0.1		$\Omega$
SW Current Limit	$V_{PWM} = 5$ , (Sinking) (Note 5)		9		A
	$V_{PWM} = 0$ , (Sourcing) (Note 5)		9		A
SW Switching Frequency	$V_{PWM} = 0$ to 2V, 50% Duty Cycle			1.2	MHz
SW Maximum Duty Cycle	$V_{SP} = 7.5V$ , $V_{PWM} = 2V$ , $C_{SW} = 100nF$ , $f_{SW} = 3.3KHz$ , Note 4		99.5		%
SW Rise/Fall Time	$V_{PWM} = 0$ to 5V		20		ns
PWM Pulse Width	$V_{PWM} = 0$ to 2V, High or Low Pulse	200			ns
PWM to SW Delay Time Rising	$V_{PWM} = 0$ to 5V		70		ns
PWM to SW Delay Time Falling	$V_{PWM} = 5$ to 0V		70		ns
Thermal Shutdown Temperature	$T_J$ Rising, Hysteresis = 20°C (Note 5)		160		°C

#### Notes:

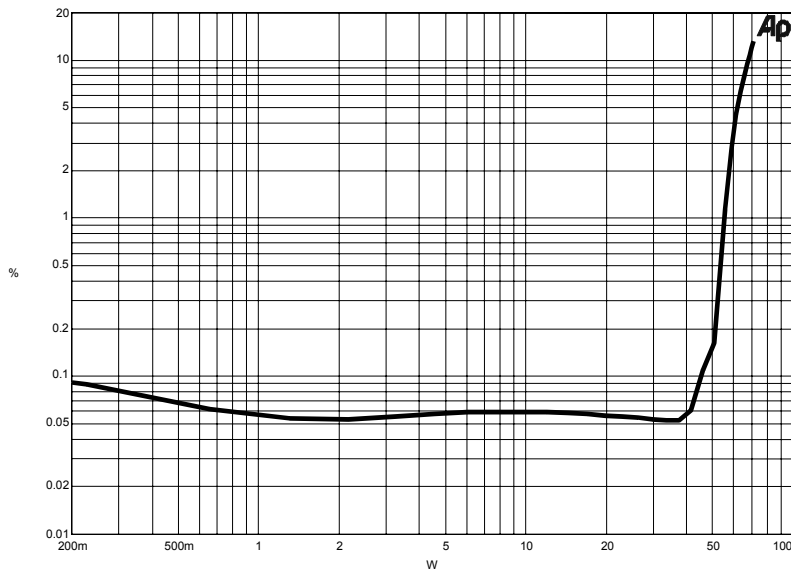
- Exceeding these limits may damage device.
  - The device is not guaranteed to function outside its operating range.
  - Measured with heat sink soldered to approximately 1" square of 1 Oz. Copper.
  - SW drives low for 1.5 $\mu s$  every 300 $\mu s$  to charge the BS to SW capacitor.
- Guaranteed by design; not production tested.

Figure 2: MP8040 Block Diagram



## Typical Operating Characteristics

Figure 3: THD+N vs. Output Power ( $V_{SP}=24V$ ) Bridged Output into  $4\Omega$  (Using closed loop circuit)



### Typical Operating Characteristics (Circuit of Figure 4, $T_A=25^\circ\text{C}$ Unless Otherwise Specified)

Figure 4: Delay Time, SP Falling ( $V_{SP}=8\text{V}$ )

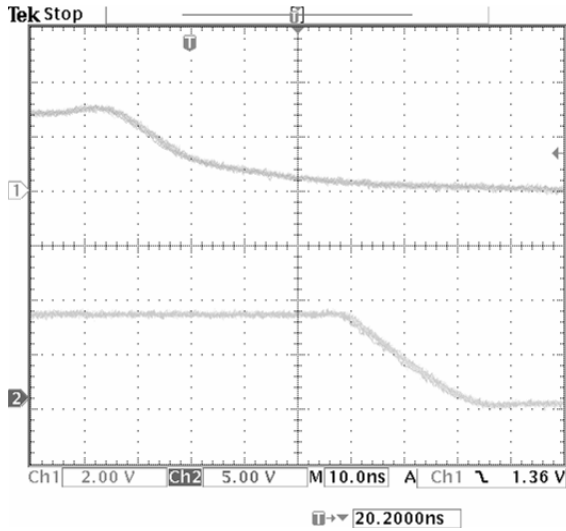


Figure 5: Delay Time, SP Rising ( $V_{SP}=25\text{V}$ )

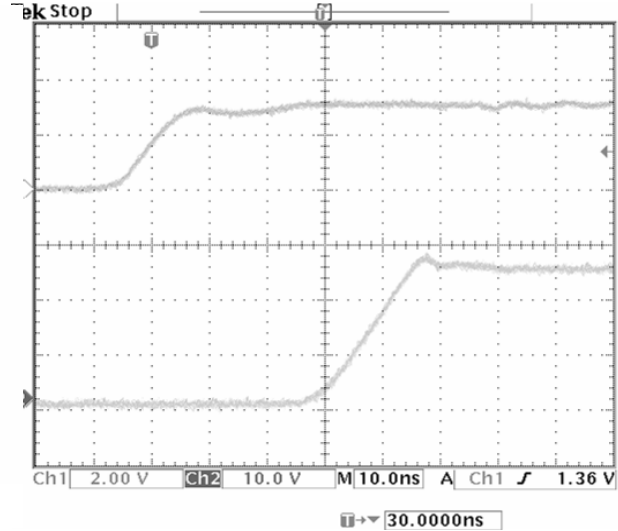


Figure 6: Delay Time, SP Rising ( $V_{SP}=8\text{V}$ )

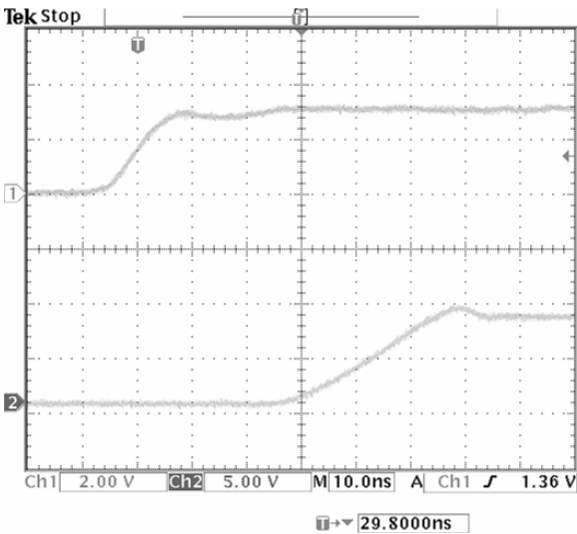
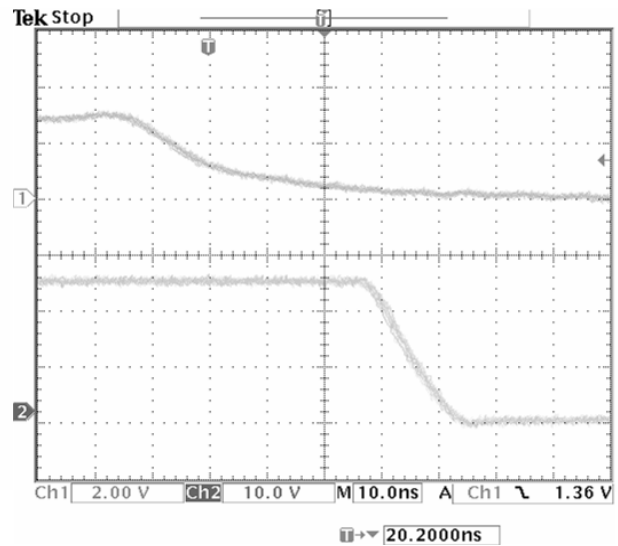


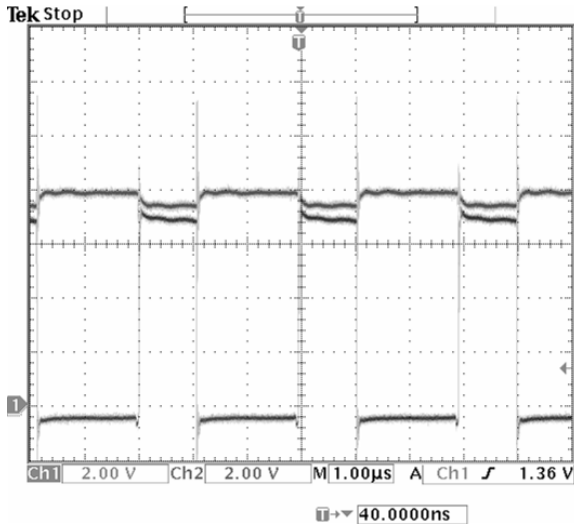
Figure 7: Delay Time, SP Falling ( $V_{SP}=25\text{V}$ )



### Typical Operating Characteristics (Circuit of Figure 4, $T_A=25^\circ\text{C}$ Unless Otherwise Specified)

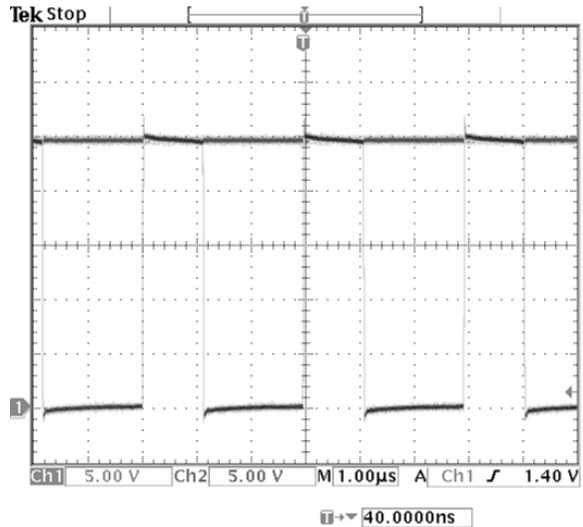
**Figure 8: Switch Waveform**  
( $V_{SP}=8\text{V}$ , 4.5A Sourcing)

1:  $V_{SP}$       2:  $V_{SW}$



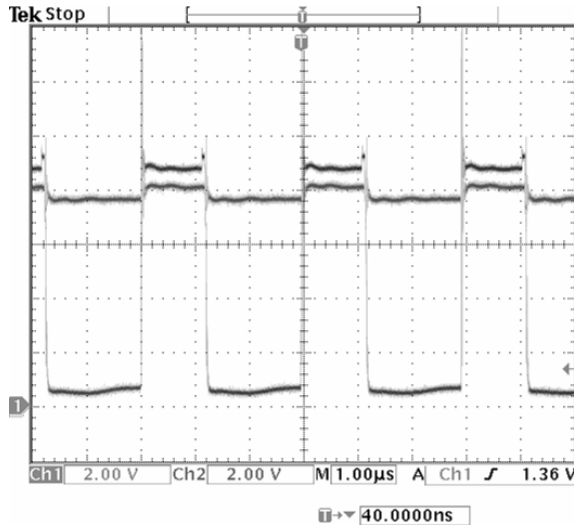
**Figure 9: Switch Waveform**  
( $V_{SP}=25\text{V}$ , 4.5A Sinking)

1:  $V_{IN}$       2:  $V_{SW}$



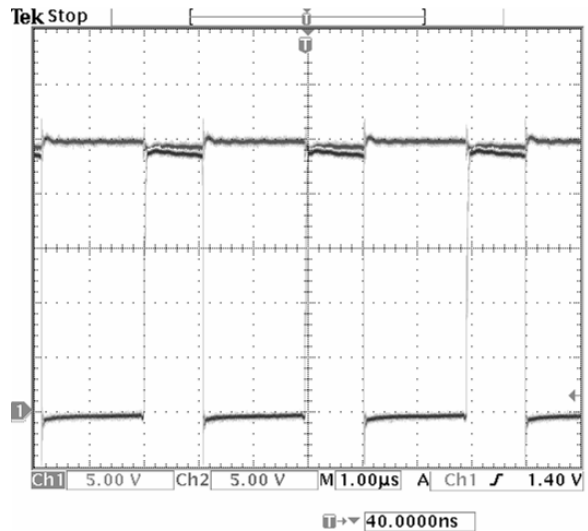
**Figure 10: Switch Waveform**  
( $V_{SP}=8\text{V}$ , 4.5A Sinking)

1:  $V_{IN}$       2:  $V_{SW}$

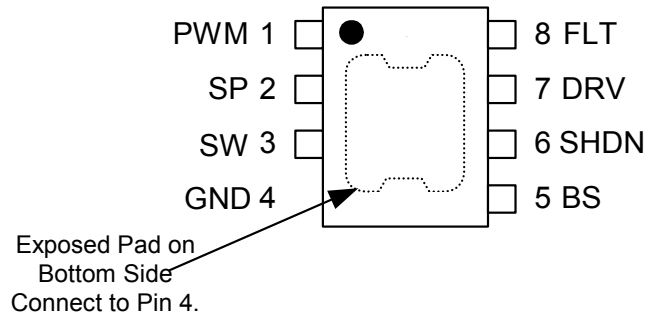


**Figure 11: Switch Waveform**  
( $V_{SP}=25\text{V}$ , 4.5A Sourcing)

1:  $V_{SP}$       2:  $V_{SW}$



### Pin Description



**Table 1: Pin Designators**

Number	Name	Function
1	PWM	Driver Logic Input. Drive PWM with the signal that controls the MP804x output. Drive PWM high to turn on the high-side switch; drive PWM low to turn on the low-side switch.
2	SP	Power Supply Input. Connect SP to the positive side of the input power supply. Bypass SP to GND as close to the IC as possible.
3	SW	Switched Output. SW is the power output of the MP804x. Connect the output LC filter to SW. SW is valid approximately 100µs after SP goes high.
4	GND	Ground. (Note: Connect the exposed pad on bottom side to Pin 4).
5	BS	Bootstrap Supply. BS powers the high-side gate of the MP804x. Connect a 0.1µF or greater capacitor between BS and SW.
6	SHDN	Shutdown Input. SHDN enables/disables the MP804x. Drive SHDN low to turn on the MP804x, drive it high to turn it off. If not used connect SHDN to GND.
7	DRV	Gate Drive Supply Bypass. The voltage at DRV is supplied from an internal regulator from SP. DRV powers the internal circuitry and internal MOSFET gate drives. Bypass DRV to GND with a 0.1µF to 10µF capacitor.
8	FLT	Fault Output. A low output at FLT indicates that the MP804x has detected a fault and has shutdown. Connect FLT to DRV through a 100KΩ resistor.

## Detailed Description

The MP804x is a general purpose, power driver. It takes a logic input and drives a half bridge comprised of 0.1Ω high-side and low-side n-channel MOSFET switches. It operates at frequencies up to .1.2MHz, DC supply voltage as high as 25V, and peak output current as high as 9A. Figure 1 shows the MP804x block diagram.

### SW Output

The SW output drives the load. It is controlled by the logic input signal at PWM. When the signal at PWM is a logic high (above 2V), the high-side switch is turned on. When the signal at PWM is low (less than 0.4V), the low-side switch is turned on.

The MP804x uses internal n-channel MOSFETs for both the high-side and low-side switches. The high-side MOSFET gate drive is powered from the voltage between SW and BS, allowing BS to rise above the SP input voltage to power the high-side MOSFET. To do this a bootstrap capacitor is connected between SW and BS. When the low-side switch is on, the capacitor is internally charged from the voltage at DRV, which is also internally generated. There is a dead time region (typically 40ns) where both the upper and lower switches are off (see Figure 12).

Both the high-side and low-side switches have internal current limits to prevent failure due to excessive load current. Once current limit is

reached, both output switches are turned off, and the fault output is asserted (driven low). **Shutdown**

The MP804x includes a 1μA shutdown mode. When SHDN is high, both output switches are turned off and the input current drops to 1μA. When the MP804x is shutdown, the internally generated voltage at DRV drops to 0V, and the fault output (FLT) is asserted (driven low). If the shutdown mode is not used, connect SHDN directly to GND.

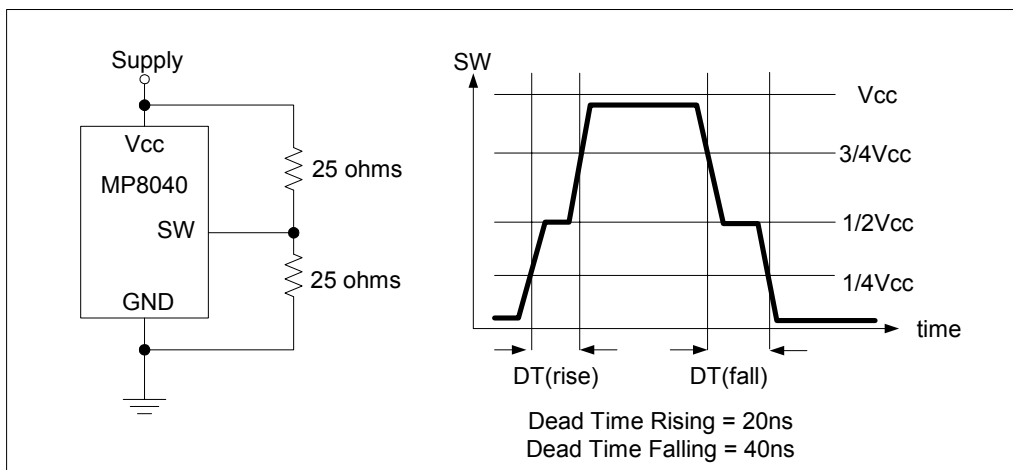
### Fault Output

The MP804x includes a fault indicator output (FLT). The MP8040 detects faults due to over-current (>9A), over-temperature (>160°C), under-voltage at SP (<6.5V), or if the part is disabled. Connect FLT to DRV or to an external voltage up to 6V through a 27KΩ or greater resistor. When any of the 3 fault conditions are detected, both output switches are turned off and the SW output is high-impedance.

### Thermal Shutdown

The MP804x includes a thermal overload protection circuit. If the die temperature rises above 160°C, the output switches are turned off and the fault output is asserted. Once the thermal overload circuit is tripped, the die temperature must drop below 140°C before automatically restarting.

Figure 12: Dead time



### Application Circuits

Figure 13: Single Ended Audio Amplifier

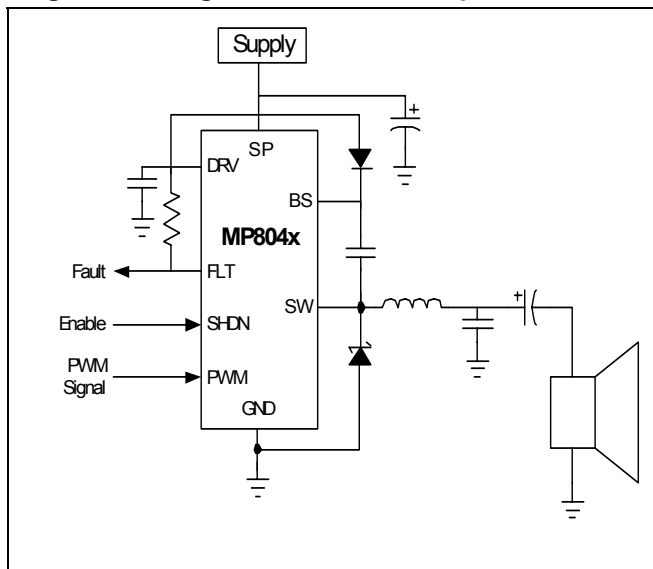


Figure 14: General Purpose DC to DC Converter

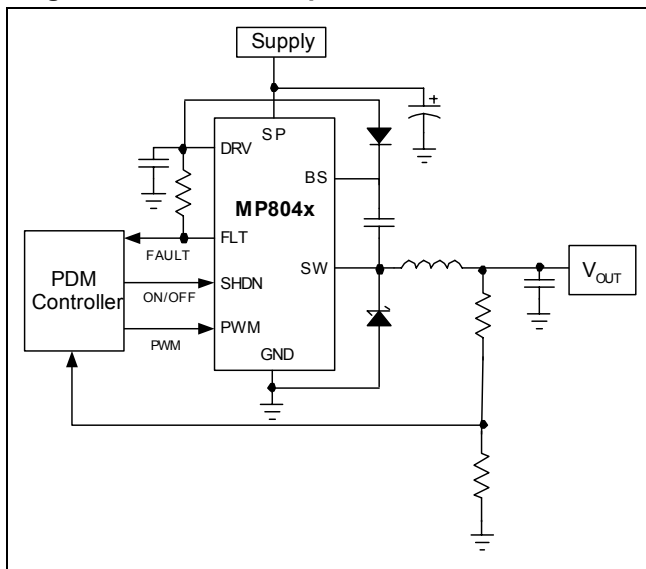


Figure 15: 80W Full Bridge Audio Amplifier

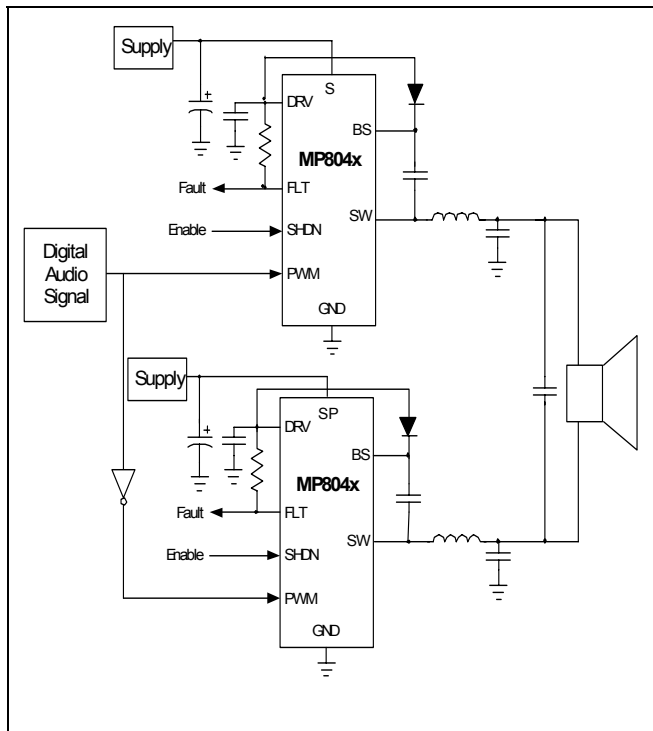
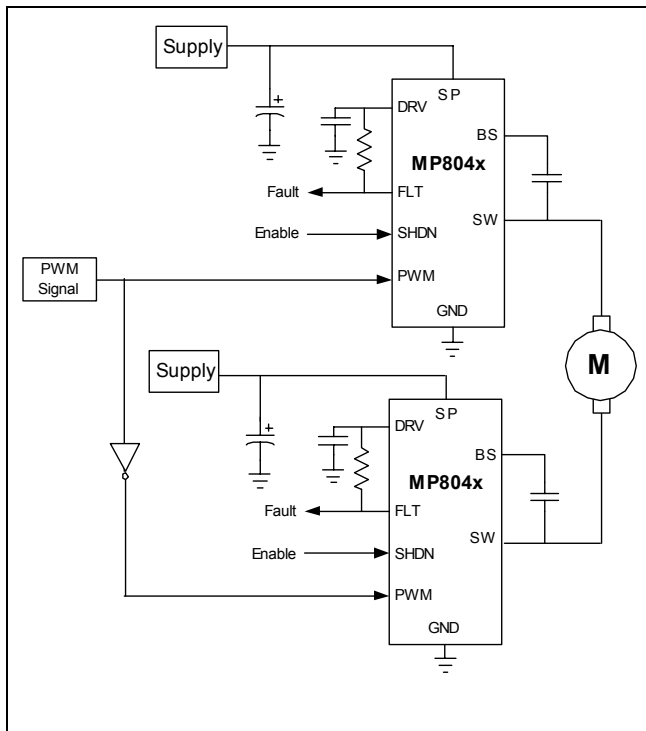


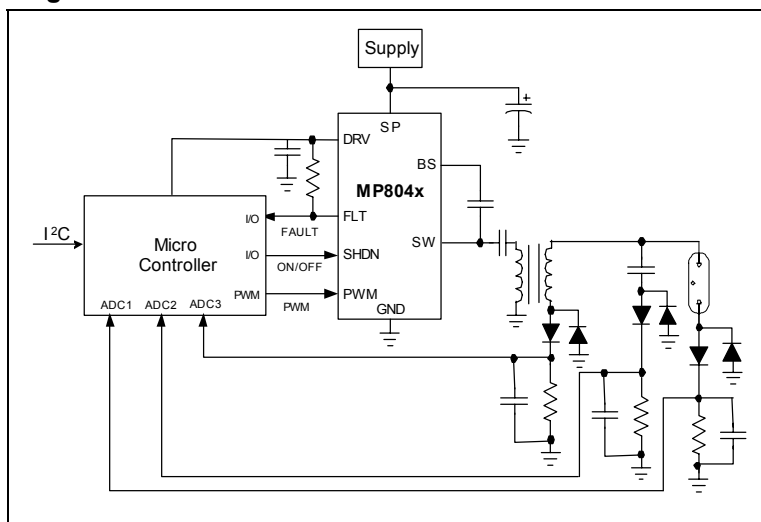
Figure 16: Full Bridge Motor Driver





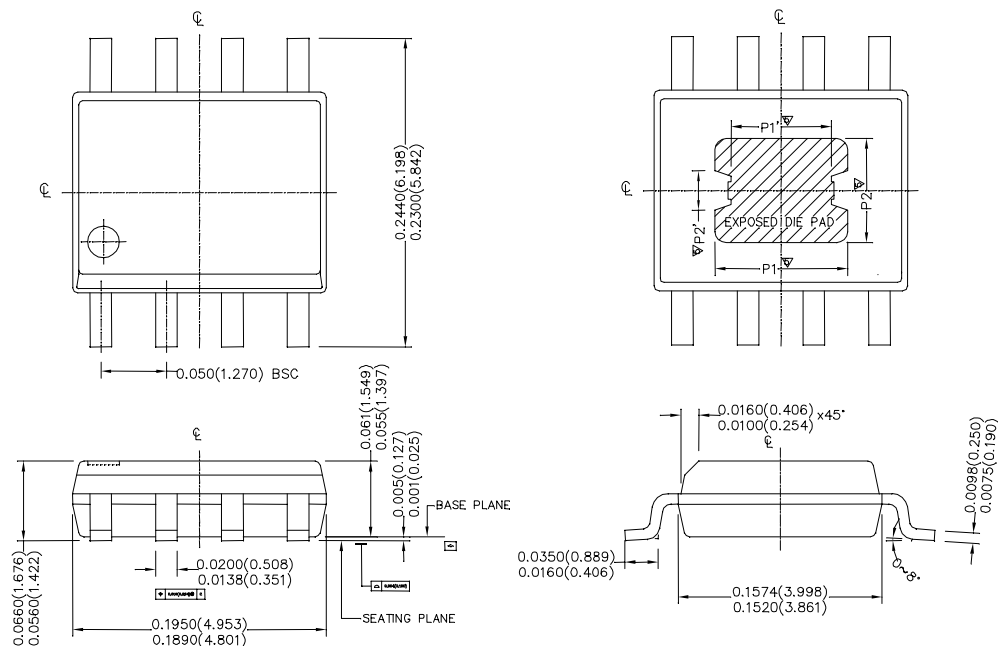
### Application Circuits Continued

Figure 17: CCFL Driver Circuit



### Packaging

#### SOIC8 with Exposed Pad



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